REMARKS

Claims 1 to 20 are pending.

Compliance of Claims with 35 U.S.C. §102

The Office Action indicates that claims 1-20 are anticipated by Grove "Performance Modeling of Message-Passing Parallel Programs" by Grove, Duncan A. and are therefore not patentable according to 35 USC § 102(b). The Applicant submits that Grove fails to disclose features recited in the claims and that the pending claims are therefore not anticipated by Grove.

The Grove Reference

Grove is a thesis that, as understood, is primarily concerned with modeling a parallel computing network in abstract terms. Grove is generally not concerned with the specific technology used to connect a CPU to a network interface. At the conclusion of section 1.2 on page 5 Grove says:

> "For the purposes of performance modelling, the only information about the communication network that is really necessary is how fast processors can communicate with each other. Therefore, regardless of the network topology that actually connects processors in a parallel computer, all types of communication network can simply be viewed as collection of processors and memories connected by "some" interconnect, along with a performance function that describes how fast messages can travel between various processors under various circumstances. Likewise, the processors can be considered as black boxes capable of computing at a certain speed, thereby abstracting over the details of superscalar functional units, pipelining, vectorising, cache behaviour, and the like. *This abstract view of processing and communication is used for the rest of this thesis.*" (Emphasis added.)

Therefore, references in Grove to 'interconnect' describe an abstract pathway by way of which data can be communicated between abstract processors.

Claim 1

Pending claim 1 recites a method for communicating data comprising "placing the data on a full-duplex packetized interconnect directly connecting a CPU of the first computer node to a network interface connected to the inter-node communication network." The term "packetized

interconnects" is explicitly defined in the Specification at paragraph [0020]. The term refers to interconnects which use memory access semantics. The Applicant submits that claim 1 is to be examined using this definition of "packetized interconnects" since, when the meaning of a term is provided in the Specification, the claims should be examined using that meaning (see MPEP §2111.01-IV and §2173.05(a)-I).

The Applicant submits that Grove fails to disclose "placing the data on a full-duplex packetized interconnect directly connecting a CPU of the first computer node to a network interface connected to the inter-node communication network" as recited in claim 1. Grove, as understood, does not specify any particular technology for interconnects or disclose a "full-duplex packetized interconnect directly connecting a CPU of the first computer node to a network interface connected to the inter-node communication network". Nor does Grove, as understood, refer to "memory access semantics".

The Examiner cites Grove section 4.6, page 143, lines 32-34, which states that "Physically, many machines (including all three of the machines benchmarked here) have full-duplex network links." The Applicant submits that by "network links" in this context, Grove is referring to the links used to connect one node to another on a network (i.e. inter-node links), not to the interconnect between a CPU and network interface within a node. To the best of the Applicant's knowledge, all three benchmarked systems that Grove mentions utilize traditional half-duplex bus technology (namely PCI or PCI-X) between the CPU and network interface.

The Applicant submits that Grove does not address the issue of intra-node connections between a CPU and network interface and does not disclose a full-duplex "packetized interconnect" directly connecting a CPU to a network interface as claimed in claim 1. Therefore the Applicant submits that Grove fails to anticipate claim 1.

Claim 2

Pending claim 2 recites a method according to claim 1 wherein "the network interface and the CPU are the only devices configured to place data on the packetized interconnect." Claim 2 depends on claim 1 and is submitted to patentably distinguish Grove for at least this reason.

Furthermore, the Applicant submits that Grove fails to disclose the features recited in claim 2. The Examiner refers to Grove section 3.4.1, page 63, lines 29 – 32, which relates to the impact of disk I/O or virtual memory access. Neither this passage nor the surrounding material concerns packetized interconnects or discloses a packetized interconnect wherein "the network interface and the CPU are the only devices configured to place data on the packetized interconnect" as claimed in claim 2. The Applicant submits that the cited passage is not relevant to the subject matter of claim 2.

The Examiner also refers to Grove section 4.4.1, page 118, lines 27 - 29, which relates to the QsNet inter-node communication network of the APAC NF system. This passage describes how the processing of network communication can be offloaded to a QsNet communication processor thus reducing the workload on a main CPU. The Applicant submits that the cited passage is not relevant to the subject matter of claim 2.

The Examiner also refers to Grove section 4.4.1, page 118, lines 35-37, which relates to the PBS scheduling application's ability to assign processes to a dedicated partition of CPUs. The Applicant submits that this passage does not disclose packetized interconnects and, in particular, does not disclose a packetized interconnect in which a CPU and network interface are the only devices configured to place data on the packetized interconnect.

Therefore, claim 2 is submitted ti distinguish Grove.

Claims 3 - 8

Pending claims 3 -8 depend on claim 1 (directly or indirectly) and are submitted to patentably distinguish Grove for at least this reason.

Claim 9

Pending claim 9 recites a method according to claim 8 wherein "the link layer packet headers comprise InfiniBand™ link layer packet headers." Pending claim 9 indirectly depends on claim 1 and is submitted to patentably distinguish Grove for at least this reason.

Furthermore, the Applicant submits that Grove does not make mention of InfiniBand™ at any point in his thesis and does not disclose the claimed feature. The Office Action indicates that Grove discloses the feature of claim 9 at section 4, page 117, lines 28 - 34 and page 118, lines 1 - 8. This description of the Orion computing system contains no reference to packet encapsulation or to InfiniBand™. The Applicant submits that the cited quote is not relevant to the subject matter of claim 9. Therefore, claim 9 is submitted to be not anticipated by Grove.

Claim 10

Pending claim 10 depends on claim 1 and is submitted to patentably distinguish Grove for at least this reason.

Claim 11

Pending claim 11 recites a compute node for use in a multi-compute-node computer system comprising "a dedicated full-duplex packetized interconnect directly coupling the CPU to the network interface." For the same reasons set out in relation to claim 1 above, the Applicant submits that Grove fails to anticipate claim 11.

Claim 12

Claim 12 recites a compute node according to claim 11 wherein "the dedicated packetized full-duplex interconnect is not shared by any devices other than the CPU and the network interface." Claim 12 depends on claim 11 and is submitted to patentably distinguish Grove for at least this reason.

Furthermore, the Applicant submits that Grove fails to disclose the features recited in claim 12. The Examiner cites Grove section 3.4.1, page 63, lines 15 – 17, which relates to code having dedicated access to the CPU and memory, and to section 3.4.1, page 63, lines 29 – 32, which relates to the impact of disk I/O or virtual memory access. Neither of these cited passages, nor the surrounding material, concern packetized interconnects or disclose a packetized interconnect that is not shared by any devices other than a CPU and a network interface. The Applicant submits that the cited passage does not disclose the subject matter of claim 12.

The Examiner cites Grove section 4.4.1, page 118, lines 27 - 29, which relates to the QsNet inter-node communication network of the APAC NF system, and to section 4.4.1, page 118, lines 35-37, which relates to the PBS scheduling application's ability to assign processes to a dedicated partition of CPUs. The Applicant submits that the cited passage does not disclose the subject matter of claim 12.

The Examiner cites Grove section 4.6, page 144, lines 11-13. This section of Grove relates to the full-duplex nature of certain inter-node links. The Applicant submits that this passage does not disclose a packetized interconnect that is not shared by any devices other than the CPU and the network interface as claimed in claim 12.

The Applicant submits that claim 12 is not anticipated by Grove because Grove fails to disclose the features recited in claim 12.

Claim 13

Claim 13 recites a compute node according to claim 11 comprising "a facility configured to allocate eager protocol buffers in the memory and to automatically signal to one or more other compute nodes that the eager protocol buffers have been allocated." Claim 13 depends from claim 11 and is submitted to patentably distinguish Grove for at least this reason.

Furthermore, the Applicant submits that Grove does not disclose the features recited in claim 13. Grove, as understood, mentions the eager protocol in only three passages. These passages can be found at: section 4.5.1, page 131, lines 7 - 12 (as noted by the Examiner), section 4.5.3, page 140, lines 24 - 29, and section 4.5.3, page 143, lines 11 - 17. None of these passages disclose the allocation of eager protocol buffers in memory or "automatically signal to one or more other compute nodes that the eager protocol buffers have been allocated" as claimed in claim 13. Therefore, the Applicant submits that claim 13 is not anticipated by Grove.

Claim 14

Claim 14 recites a compute node according to claim 13 comprising "a facility configured to automatically associate memory protection keys with the eager protocol buffers and a facility

configured to verify memory protection keys in incoming eager protocol messages before writing the incoming eager protocol messages to the eager protocol buffers." Claim 14 directly depends on claim 13 and indirectly depends on claim 11 and is submitted to patentably distinguish Grove for at least these reasons.

Furthermore, the Applicant submits that Grove makes no mention, either in the passages the Examiner has cited or in any other passage, of memory protection keys associated with the eager protocol. Therefore, the Applicant submits that claim 14 is not anticipated by Grove.

Claims 15 - 20

Claims 15 - 20 depend from claim 11 and are submitted to patentably distinguish Grove for at least this reason.

Conclusion

For the reasons above, the Applicant submits that Grove fails to anticipate any of claims 1 to 20. The Applicant submits that claims 1 to 20 are patentable over Grove and respectfully requests reconsideration and allowance of this application. The Examiner is requested to contact the undersigned to arrange an interview if any questions, formalities, or other outstanding issues should be addressed before the application is allowed.

Respectfully submitted,
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